What is claimed is:

1. An analog delay locked loop comprising:

an analog delay line having an associated minimum delay;

an input for receiving a reference clock signal;

an output for providing a delayed clock signal; and

means for controlling the delay through the analog delay line such that the delay is initialized at or near the minimum delay.

2. The analog delay locked loop according to claim 1 in which the delay through the analog delay line only increases initially, independent of the phase relationship between the reference and delayed clock signals.

3. The analog delay locked loop according to claim 1 in which the means for controlling the delay through the analog delay line comprises a phase detector for receiving the reference and delayed clock signals and for providing output control signals.

4. The analog delay locked loop according to claim 3 in which the delay through the analog delay line only increases initially, independent of the output control signals of the phase detector.

5. The analog delay locked loop according to claim 2 in which the magnitude of incremental delay increases are proportional to the phase difference between the reference and delayed clock signals.

6. The analog delay locked loop according to claim 3 in which the delay through the analog delay line is increased or decreased after the rising edge of the delayed clock signal is ahead of the rising edge of the reference clock signal by a minimum time.

7. The analog delay locked loop according to claim 3 in which the phase detector further comprises means for generating a first indication that the delay is to be increased.

8. The analog delay locked loop according to claim 3 in which the means for controlling the delay through the analog delay line further comprises a fast/slow latch circuit coupled to the phase detector.

9. The analog delay locked loop according to claim 8 in which the fast/slow latch circuit includes an output for generating a positive going variable width signal for indicating that the delay through the analog delay line should be decreased.

10. The analog delay locked loop according to claim 8 in which the fast/slow latch circuit includes an output for generating a positive going variable width signal for indicating that the delay through the analog delay line should be increased.

11. The analog delay locked loop according to claim 8 in which the fast/slow latch circuit includes an output for generating a negative going variable width signal for

indicating that the delay through the analog delay line should be increased.

12. The analog delay locked loop according to claim 8 in which the fast/slow latch circuit includes means for generating first, second, and third output control signals having a width dependent upon the phase difference between the reference clock signal and the delayed clock signal.

13. The analog delay locked loop according to claim 8 in which the fast/slow latch circuit includes means for generating three variable width signals, two positive signals having a designated minimum high time and one negative signal having a designated minimum low time.

14. The analog delay locked loop according to claim 8 in which the means for controlling the delay through the analog delay line only responds to a negative going variable width signal generated by the fast/slow latch circuit until a first positive going signal generated by the fast/slow latch for indicating that the delay though the analog delay line should be increased goes positive for a first time.

15. The analog delay locked loop according to claim 14 in which the fast/slow latch circuit includes means for generating a second positive going signal for indicating that the delay through the analog delay line should be decreased.

16. The analog delay locked loop according to claim 15 in which, after the first occurrence of the first positive going signal, the means for controlling the delay through the analog delay line only responds to said first and second positive going signals.

17. The analog delay locked loop according to claim 8 in which the means for controlling the delay through the analog delay line comprises means for generating a first magnitude of control voltage adjusting current until a positive going signal generated by the fast/slow latch for indicating that the delay should be increased goes positive for a first time and, after that, for generating a second magnitude of adjusting current.

18. The analog delay locked loop according to claim 3 further comprising a reset circuit for preventing a false control signal from being generated by the phase detector.

19. The analog delay locked loop according to claim 1 further comprising a reset circuit that causes the analog delay locked loop to be reset as soon as the reference clock starts after having been off for a predetermined minimum time.

20. The analog delay locked loop according to claim 1 in which the means for controlling the delay through the analog delay line further comprises first and second charge integrating capacitors.

21. The analog delay locked loop according to claim 20 further comprising a reset circuit having a reset time sufficient for the charge integrating capacitors to reset to an initializing value independent of the width of an input reset signal.

22. The analog delay locked loop according to claim 1 in which the means for controlling the delay through the analog delay line comprises three different levels of DC bias current depending on whether the analog delay locked loop is on with the reference clock signal running, on with the reference clock signal not running, or off.

23. The analog delay locked loop according to claim 1 in which the means for controlling the delay through the analog delay line comprises:

a phase detector having inputs for receiving the reference clock signal and the delayed clock signal;

a fast/slow latch having three output control signals coupled to the phase detector; and

a delay voltage control circuit having an input coupled to the fast/slow latch and an output coupled to the analog delay line and at least one integrating capacitor.

24. An analog delay locked loop comprising:

a clock input;

a sync output;

a phase detector coupled to the clock input and sync output;

a fast/slow latch for generating three output control signals coupled to the phase detector;

a delay voltage control circuit coupled to the fast/slow latch having first and second outputs;

first and second integrating capacitors respectively coupled to the first and second outputs of the delay voltage control circuit;

a voltage controlled analog delay line having an input coupled to the clock input, first and second control terminals respectively coupled to the first and second outputs of the delay voltage control circuit, and an output coupled to the sync output through a fixed delay line.

25. A method for operating an analog delay locked loop including an analog delay line having an associated minimum delay, an input for receiving a reference clock signal, an output for providing a delayed clock signal, the method comprising voltage controlling the delay through the analog delay line such that the delay is initialized at or near the minimum delay and initially only increasing the delay independently of the phase relationship between the reference and delayed clock signals.